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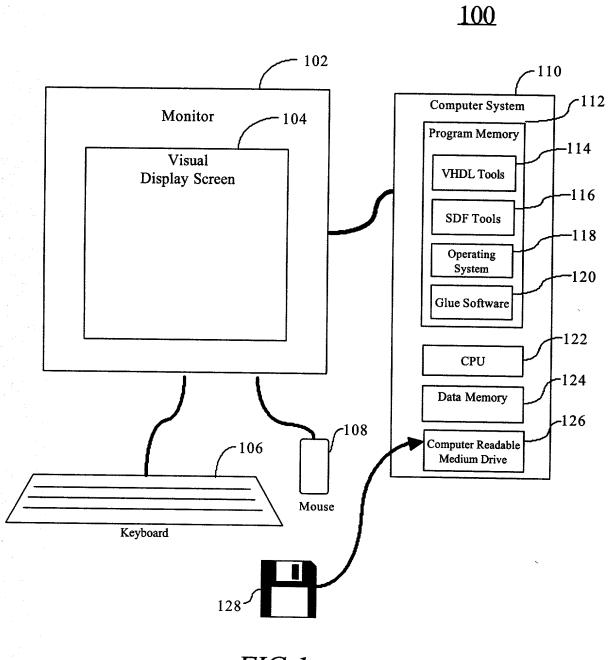


FIG 1

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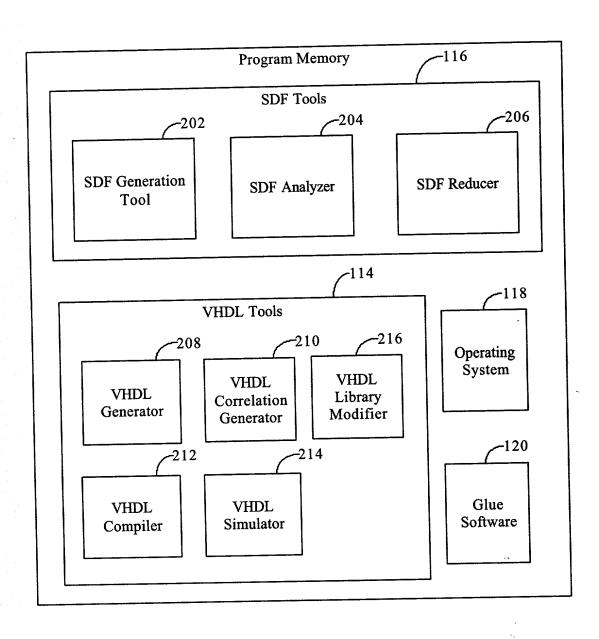


FIG 2

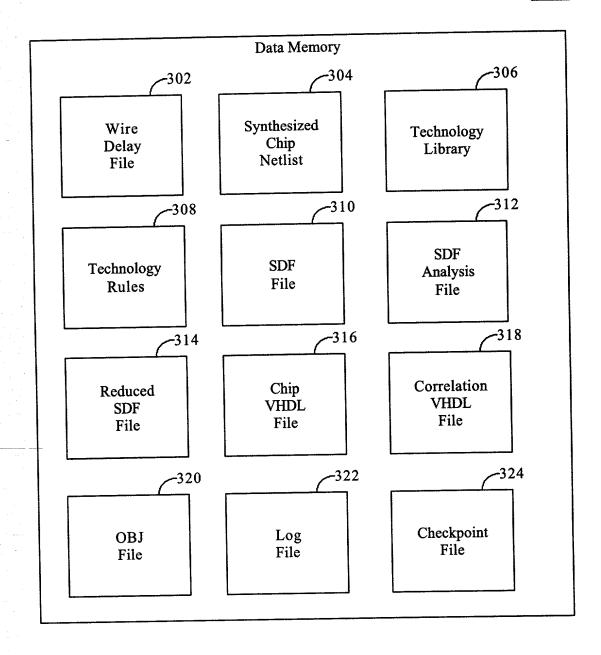


FIG 3

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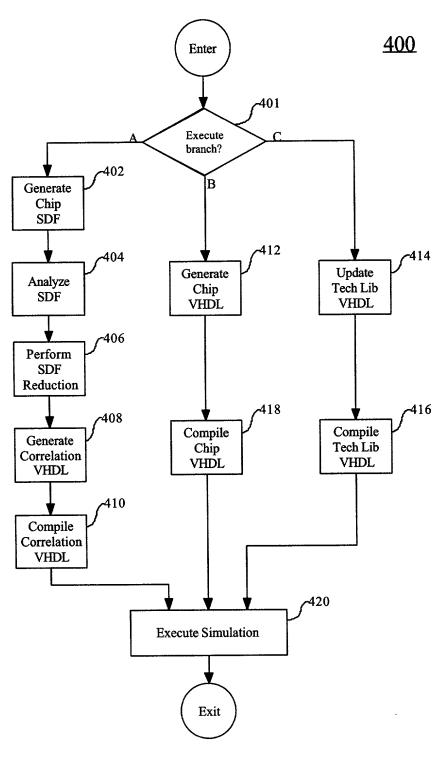


FIG 4

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<u>402</u>

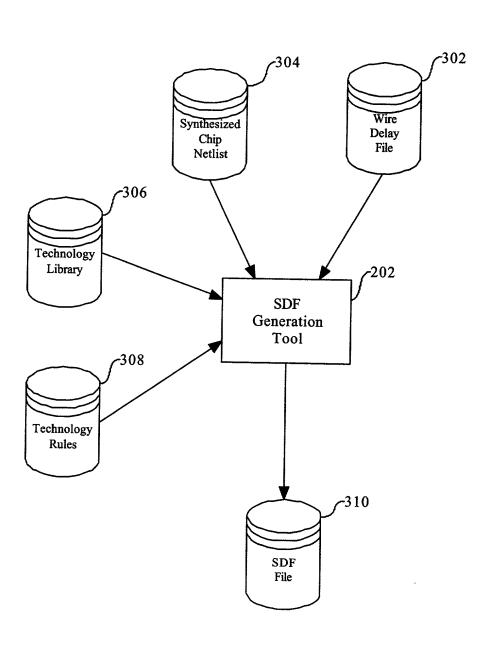
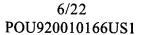
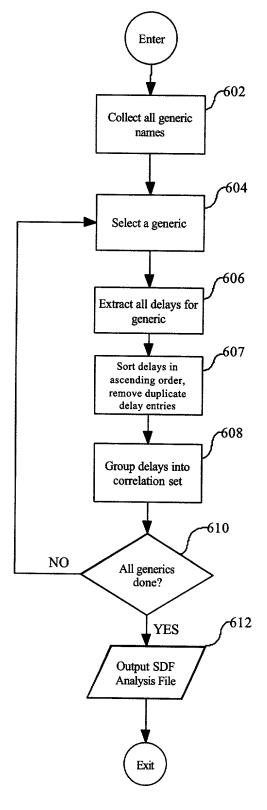


FIG 5





404

FIG 6



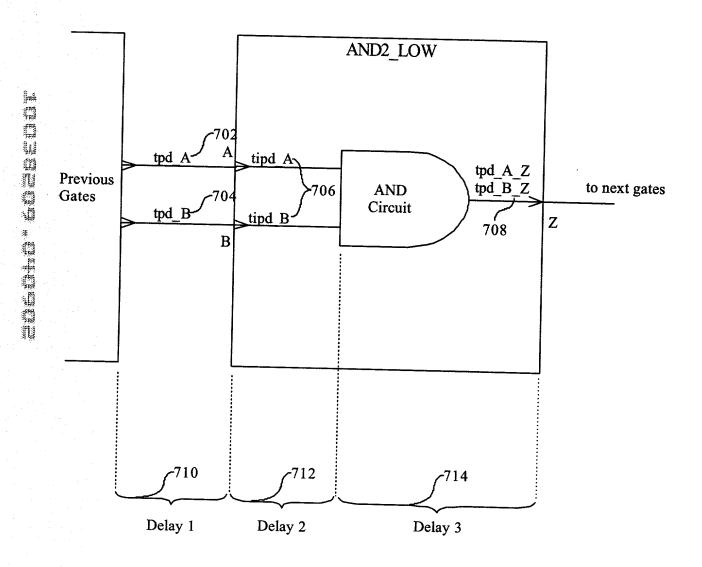


FIG 7

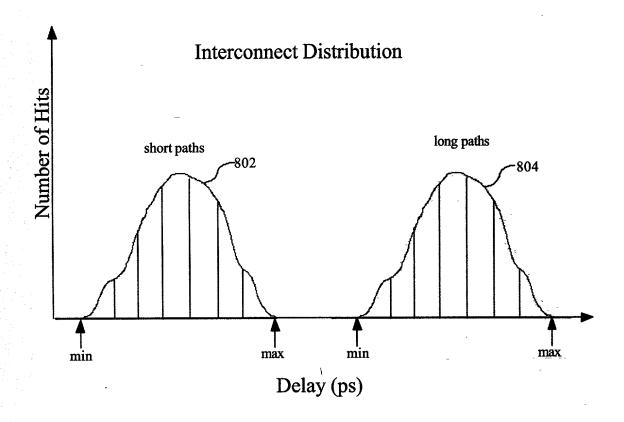


FIG 8

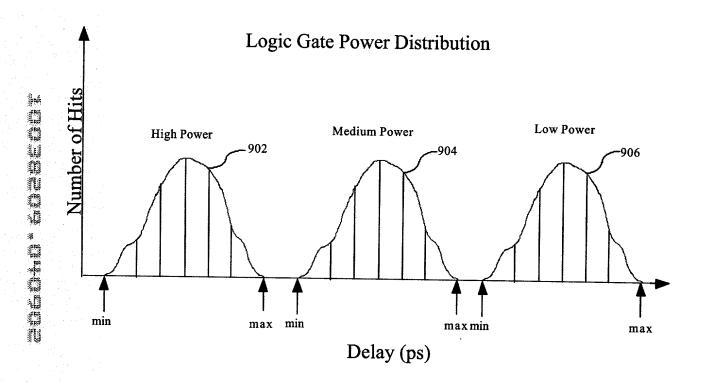


FIG 9

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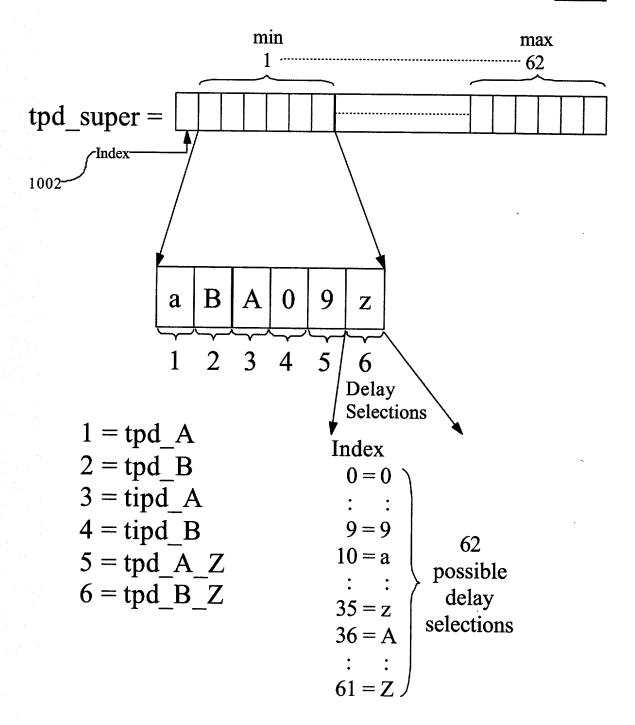


FIG 10

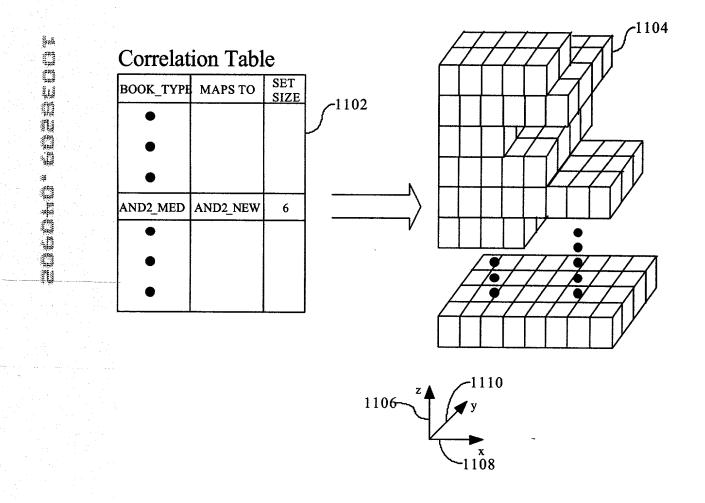
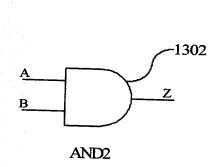


FIG 11

CHAR POSITION (0 OFFSET)	CHAR VALUE	Correlation Set (x')	Entry Position (y')	Slot Offset (x")
0	1	N/A	N/A	NΑ
1	4	1	5th	1st
2	Χ	1	60th	2nd
3	а	1	11th	3rd
4	m	1	26th	4th
5	р	1	29th	5th
6	1	1	25th	6th

FIG 12



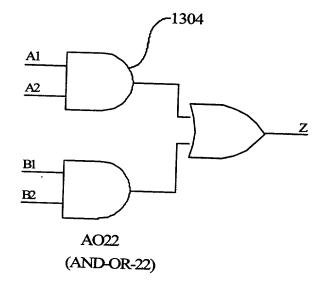


FIG 13

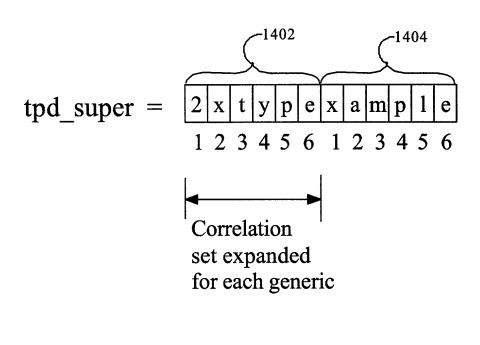


FIG 14

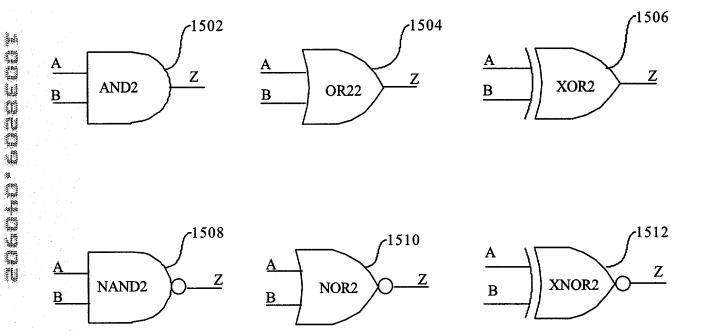
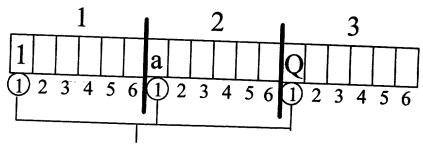


FIG 15

1600



tpd\_A positions for AND2 gate

### Encode as:

	DELAY		tpd A		
	DELAY	1	2	3	1
	-0.500 ns	0	0	0	ı
j	-0.499 ns	0	0	1	ı
4	· •	-			L
1	• -	• .	<b>十 -</b> こ	r = 1	۲
١	+237.826 ns	Z	Z	v	
L	+237.827 ns	Z	Z	7	l
				<u> </u>	

FIG 16

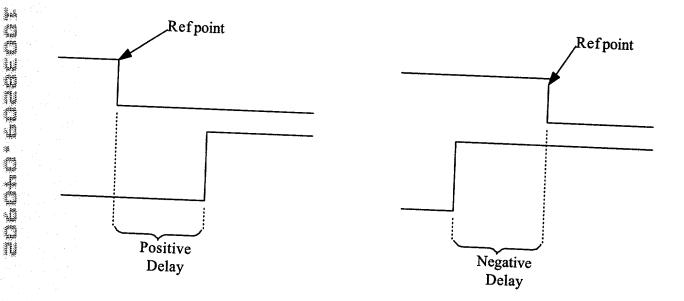


FIG 17

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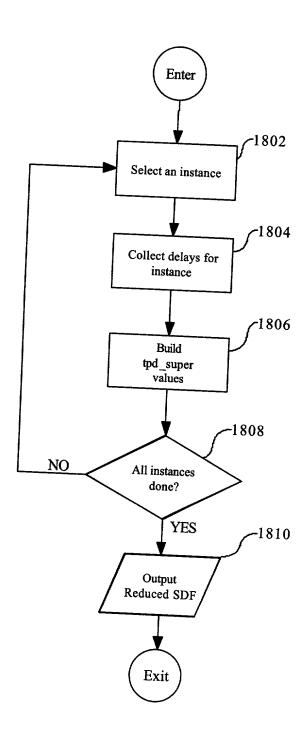


FIG 18

## <u>408</u>

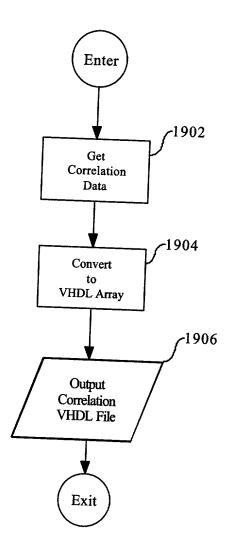


FIG 19

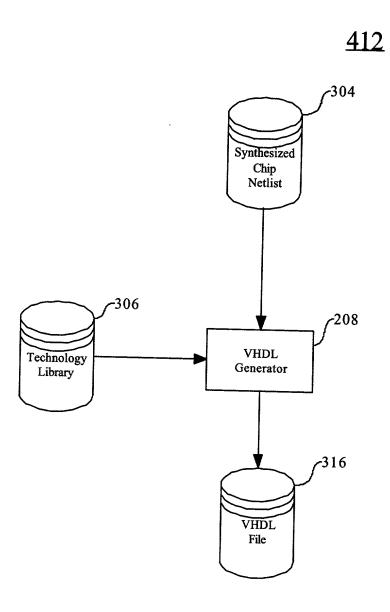


FIG 20

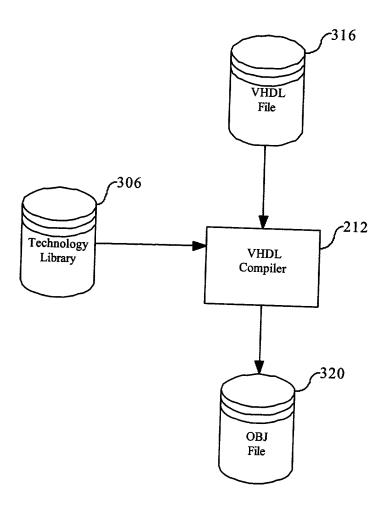


FIG 21

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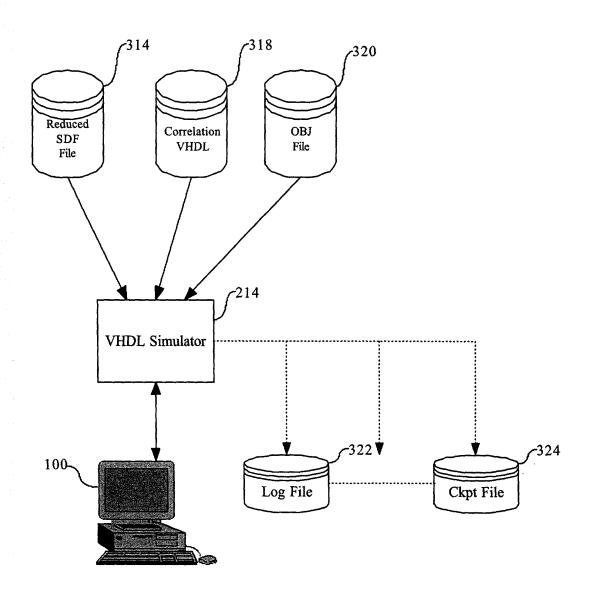


FIG 22